REMARKS

Claims 1-9 and 19-24 are pending in the present application. Claims 1, 19, and 23 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

Applicants note with appreciation that the Office Action indicates at page 12 that claims 3-5, 7, 21-22 and 24 would be allowable if rewritten in independent form. Applicants wish to defer submission of these claims, pending consideration of the present Amendment.

Claims 1, 6, 8-9, 19-20 and 23 stand rejected under 35 U.S.C. 103(a) as being anticipated by Suemura *et al.* (U.S. Patent No. 5,887,039 - hereinafter "Suemura") in view of Co, *et al.* (U.S. Patent No. 5,602,882 - hereinafter "Co). Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura in view of Co, and in further view of Sakamoto, *et al.* (U.S. Patent No. 6,557,110 - hereinafter "Sakamoto"). Reconsideration and removal of the rejections, and allowance of the claims, are respectfully requested.

In the present invention as claimed in amended independent claim 1, a "receiver phase locked loop" generates a "second plurality of non-overlapping clock signals" of "different respective phases" in response to a "received clock included in the received optical signal." The "non-overlapping clock signals" each have a "frequency that is the same as a frequency of the received clock."

In the present invention as claimed in amended independent claim 19, a "data restoration and skew compensation unit" generates "first through n-th non-overlapped clock signals" in

response to a "clock signal received on a transmission channel." The "first through n-th non-overlapped clock signals" each have a "frequency that is the same as a frequency of the received clock signal."

In the present invention as claimed in amended independent claim 23, a "method of restoring information data from data in which n-bit synchronous signals...and the n-bit information data are multiplexed and transmitted together with a clock signal in series via a transmission channel" includes a step of "generating first through n-th non-overlapped clock signals...on the basis of the clock signal." The "first through n-th non-overlapped clock signals" each have a "frequency that is the same as a frequency of the clock signal."

With regard to the rejection of independent claim 1, it is submitted that the combination of Suemura and Co fails to teach or suggest the present invention as claimed. In particular, the combination of Suemura and Co fails to teach or suggest "a receiver phase locked loop that generates a second plurality of non-overlapping clock signals of different respective phases in response to a received clock included in the received optical signal...the non-overlapping clock signals each having a frequency that is the same as a frequency of the received clock," as claimed in amended independent claim 1.

With regard to Suemera, the applicants agree with statements made in the Office Action at page 6, first paragraph, that Suemera does not disclose the non-overlapping clock signals, as claimed.

With regard to Co, the jitter attenuator of Co includes a first plurality of multi-phase clock signals 32 that are generated in response to an output of a 32 MHz external crystal oscillator (see Co, Figs. 3-4 and column 5, lines 37-39). The Co 32 MHz external crystal oscillator output signal is not a received clock, but rather is internally generated. Further, the multi-phase clocks 32 of Co are not of a frequency that is "the same as a frequency of the received clock," as claimed. Moreover, the multi-phase clocks 32 of Co are not generated in

response to the Co receive clock 11 Rx CLK.

A second plurality of clock signals of Co are the read clock signals 38, R0-R7, which are produced by dividing the filtered receive clock 20 at the output divider 38, the filtered receive clock 20 being a selected one of the multi-phase clock signals 32 (see Co, Fig. 3, column 5, lines 1-5 and 63-65). In this manner, the read clocks 38, R0-R7 operate at $1/64^{th}$ the frequency of the filtered receive clock 20 (see Co, column 5, lines 66-67). Thus, the read clocks 38, R0-R7 of Co are not of a frequency that is "the same as a frequency of the received clock," as claimed.

A third plurality of clock signals of Co are the write clock signals W0-W7 (see Co, Fig. 3). The write clock signals W0-W7 are likewise generated by dividing the receive clock 11 Rx CLK 11 by 64 at divider 26 (see Co, column 4, lines 34-40, and column 6, lines 4-5). Thus, the write clocks W0-W7, similar to the read clocks R0-R7, operate at 1/64th the frequency of the receive clock 11 Rx CLK, and are likewise not of a frequency that is "the same as a frequency of the received clock," as claimed.

With regard to the rejection of independent claim 19, it is submitted that the combination of Suemura and Co fails to teach or suggest "first through n-th non-overlapped clock signals each having a frequency that is the same as a frequency of the received clock signal," as claimed in amended independent claim 19, for reasons similar to those described above.

With regard to the rejection of independent claim 23, it is submitted that the combination of Suemura and Co fails to teach or suggest "first through n-th non-overlapped clock signals each having a frequency that is the same as a frequency of the clock signal," for reasons similar to those described above.

Accordingly, it is submitted that Suemura and Co, taken alone or in combination, fail to teach or suggest the invention set forth in independent claims 1, 19 , and 23. Since neither the Suemura reference nor the Co reference individually teaches or suggests these claimed features,

there is no way to combine the references to obtain teaching or suggestion of the claimed features, and, therefore, there is no combination of the references that teaches or suggests the invention as set forth in claims 1, 19, and 23. Accordingly, reconsideration and removal of the rejection of claims 1, 6, 8-9, 19-20, and 23 under 35 U.S.C. 103(a) based on Suemura and Co are respectfully requested.

With regard to dependent claim 2, it is submitted that Sakamoto, like Suemura and Co, fails to teach or suggest fails to teach or suggest the aforementioned features of independent claim 1. Specifically, Sakamoto likewise fails to teach or suggest "a receiver phase locked loop that generates a second plurality of non-overlapping clock signals of different respective phases in response to a received clock included in the received optical signal...the non-overlapping clock signals each having a frequency that is the same as a frequency of the received clock," as claimed. Accordingly since Suemura, Co, and Sakamoto, taken alone or in combination, fail to teach or suggest the present invention set forth in claim 2, the claim is believed to be allowable over the references. Accordingly, reconsideration and removal of the rejection of claim 2 under 35 U.S.C. 103(a) based on the combination of Suemura, Co, and Sakamoto is respectfully requested.

Closing Remarks

Entry of the above amendments and allowance of all claims are respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900, Ext. 4902
Facsimile: (617) 742-7774
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